



MS-7302 VER:1.0

CPU:

AMD M2 Athlon 64/Athlon 64 FX AM2R2

System Chipset:

AMD/ATI RS780 colay RS740

AMD/ATI SB700

On Board Chipset:

FINTEK Super I/O -- F71882

LAN -- RTL8111C(B)/RTL8101E

HD Codec -- ALC888

BIOS -- SPI ROM 8M

1394 -- JMB381

Main Memory:

DDR II X 2 (Max 4GB)

Expansion Slots:

PCI-E X 1 *1

PCI-E X 16 *1

PCI 2.2 Slot X 2

Clock Generator:

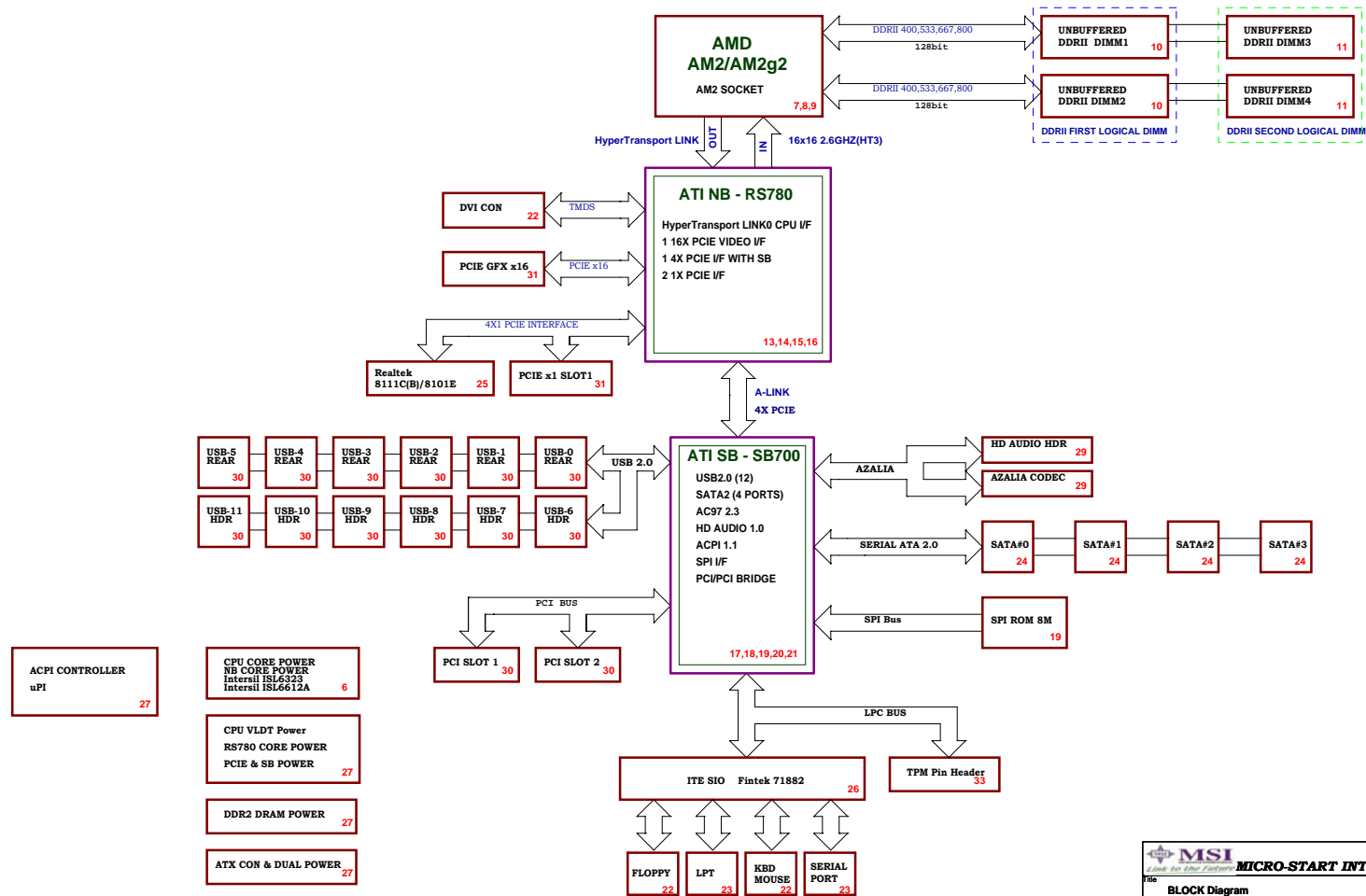
Controller--ICS9LPRS477

PWM:

INTSIL6566 3 Phase+75125

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Project RS-780 BLOCK DIAGRAM



GPIO Name	Type	Function Description	Pin	Page
PCICLK5/GPIO41	3.3V	PC1_CLK5	T3	17
REQ3#/GPIO70		PREQ#3	AE6	17
REQ4#/GPIO71		PREQ#4	AB6	17
GNT3#/GPIO72		Unused	AC6	17
GNT4#/GPIO73		Unused	AE5	17
INT#/#GPIO33		PC1_INT#	AD3	17
INTF#/GPIO33		PC1_INTB#	AC4	17
INTG#/GPIO33		PC1_INT#	AE2	17
INTH#/GPIO33		PC1_INTD#	AE3	17
LDRQ1#/GNT5#/GPIO68		Unused	AB8	17
BMREQ#/REQ5#/GPIO65		PREQ#5	AD7	17
RIB#EXT#VNT0#		RIB#	E2	18
SLP_S2/GPM0#		Unused	H7	18
GA20IN#GEVENT0#		A20GATE	Y15	18
KBRST#/GEVENT1#		KBRST#	W15	18
LPC_PME#/GEVENT3#		LPC_PME#	K4	18
LPC_SM#/#EXT#VNT1#		LPC_SM#	K24	18
S3_STATE#GEVENT5#		Unused	F1	18
SYS_RESE#/#GPM7#		FP_RST#	J2	18
WAKE#/GEVENT8#		WAKE#	H6	18
BLINK/GPM8#		Unused	F2	18
SMBALERT#/#HRMTRIP#/GEVENT2#		SMBALERT#	J6	18
SATA_ISO#/GPIO10		SB_GPIO10(Strapping)	AE18	18
CLK_REQ3#/SATA_IS1#/GPIO6		SB_GPIO6(Strapping)	AD18	18
SMARTVOLT#/SATA_IS2#/GPIO4		SB_GPIO4(Strapping)	AA19	18
CLK_REQ0#/SATA_IS3#/GPIO0		SB_GPIO0(Strapping)	W17	18
CLK_REQ0#/SATA_IS4#/FANOUT3/GPIO38		SB_GPIO38(Strapping)	V17	18
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40		SB_GPIO40(Strapping)	W20	18
SPKR/GPIO2		SPKR	W21	18
SCL0/GPOC0#		SCLK	AA18	18
SDA0/GPOC1#		SDATA	W18	18
SCL1/GPOC2#		SCLK1	K1	18
SDA1/GPOC3#		SDATA1	K2	18
DDC1_SCL/GPIO9		Unused	AA20	18
DDC1_SDA/GPIO8		SPI_WP#	Y16	18
LLB#/GPIO66		LC_SENSE	C1	18
SHUTDOWN#/GPIO5		SB_GPIO5(Strapping)	Y19	18
DDR3_RST#/GEVENT7#		Unused	G5	18
USB_OC6#/IR_TX1/GEVENT6#		OC4#	B9	18
USB_OC5#/IR_TX0/GPM5#		OC4#	B8	18
USB_OC4#/IR_TX0/GPM4#		OC3#	A6	18
USB_OC3#/IR_TX1/GPM3#		OC3#	A6	18
USB_OC2#/GPM2#		OC2#	E5	18
USB_OC1#/GPM1#		OC2#	F8	18
USB_OC0#/GPM0#		OC1#	E4	18
AZ_SDIN0/GPIO42		SDATA_IN_R	J7	18
AZ_SDIN1/GPIO43		Unused	J8	18
AZ_SDIN2/GPIO44		Unused	L8	18
AZ_SDIN3/GPIO46		Unused	M3	18

GPIO Name	Type	Function Description	Pin	Page
AZ_DOCK_RST#/GPM8#		Unused	L5	18
PS2_DAT#EC_GPIO0		Unused	H19	18
PS2_CLK#EC_GPIO1		Unused	H20	18
SPI_CS2#EC_GPIO2		Unused	H21	18
IDE_RST#/#RST#EC_GPIO3		Unused	F25	18
PS2KB_DAT#EC_GPIO4		Unused	O22	18
PS2KB_CLK#EC_GPIO5		Unused	E24	18
PS2M_DAT#EC_GPIO6		Unused	E25	18
PS2M_CLK#EC_GPIO7		Unused	O23	18
USBCLK14M_25M_48M_OSC		USB_48M_CLK	C8	18
KSO_16#EC_GPIO8		Unused	A18	18
KSO_17#EC_GPIO9		Unused	B18	18
EC_PWM0#EC_GPIO10		Unused	F21	18
SCL2#EC_GPIO11		Unused	D21	18
SDA2#EC_GPIO12		Unused	F19	18
SCL3_LV#EC_GPIO13		Unused	E20	18
SDA3_LV#EC_GPIO14		Unused	E21	18
EC_PWM1#EC_GPIO15		Unused	E19	18
EC_PWM2#EC_GPIO16		SB_GP16(Strapping)	D19	18
EC_PWM3#EC_GPIO17		Unused	E18	18
KSI_0#EC_GPIO18		Unused	G20	18
KSI_1#EC_GPIO19		Unused	G21	18
KSI_2#EC_GPIO20		Unused	D25	18
KSI_3#EC_GPIO21		Unused	D24	18
KSI_4#EC_GPIO22		Unused	C25	18
KSI_5#EC_GPIO23		Unused	C24	18
KSI_6#EC_GPIO24		Unused	B25	18
KSI_7#EC_GPIO25		Unused	C23	18
KSO_0#EC_GPIO26		Unused	B24	18
KSO_1#EC_GPIO27		Unused	B23	18
KSO_2#EC_GPIO28		Unused	A23	18
KSO_3#EC_GPIO29		Unused	C22	18
KSO_4#EC_GPIO30		Unused	A22	18
KSO_5#EC_GPIO31		Unused	B22	18
KSO_6#EC_GPIO32		Unused	B21	18
KSO_7#EC_GPIO33		Unused	A21	18
KSO_8#EC_GPIO34		Unused	D20	18
KSO_9#EC_GPIO35		Unused	C20	18
KSO_10#EC_GPIO36		Unused	A20	18
KSO_11#EC_GPIO37		Unused	B20	18
KSO_12#EC_GPIO38		Unused	B19	18
KSO_13#EC_GPIO39		Unused	A19	18
KSO_14#EC_GPIO40		Unused	D18	18
KSO_15#EC_GPIO41		Unused	C18	18
SATA_ACT#/GPIO67		SATA_LED#	W11	19
IDE_D0/GPIO15		Unused	AD24	19
IDE_D1/GPIO16		Unused	AD23	19
IDE_D2/GPIO17		Unused	AE22	19
IDE_D3/GPIO18		Unused	AC22	19

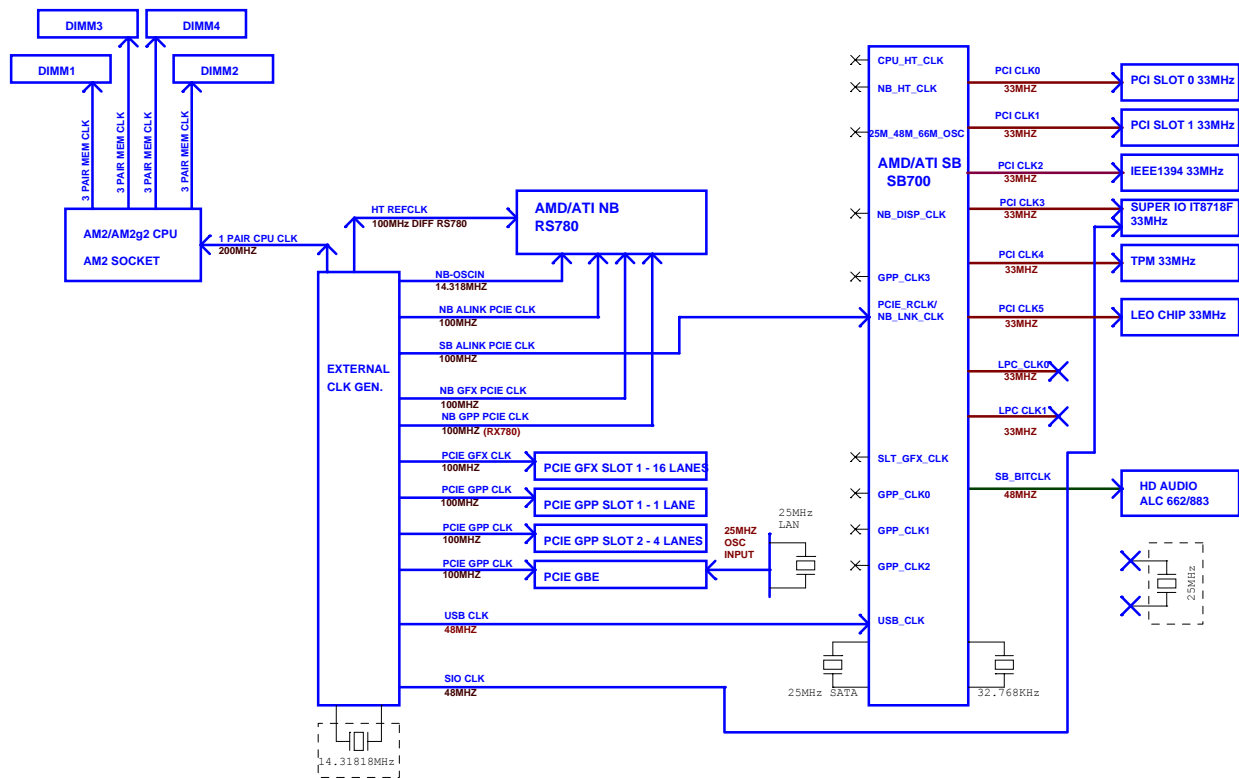
GPIO Name	Type	Function Description	Pin	Page
IDE_D4/GPIO19		Unused	AD21	19
IDE_D5/GPIO20		Unused	AE20	19
IDE_D6/GPIO21		Unused	AB20	19
IDE_D7/GPIO22		Unused	AD19	19
IDE_D8/GPIO23		Unused	AE19	19
IDE_D9/GPIO24		Unused	AC20	19
IDE_D10/GPIO25		Unused	AD20	19
IDE_D11/GPIO26		Unused	AE21	19
IDE_D12/GPIO27		Unused	AB22	19
IDE_D13/GPIO28		Unused	AD22	19
IDE_D14/GPIO29		Unused	AE23	19
IDE_D15/GPIO30		Unused	AC23	19
SPI_DI/GPIO12		SPI_DATAIN	G6	19
SPI_DO/GPIO11		SPI_DATAOUT	D2	19
SPI_CLK/GPIO47		SPI_CLK	D1	19
SPI_HOLD#/GPIO31		SPI_HOLD_L	F4	19
SPI_CS#/GPIO32		SPI_CS#	F3	19
LAN_RST#/GPIO13		CPU_PRESENT#	U15	19
ROM_RST#/GPIO14		Unused	J1	19
FANOUT1/GPIO3		Unused	M8	19
FANOUT1/GPIO48		COM_GPIO	M5	19
FANOUT2/GPIO49		Unused	M7	19
FANIN0/GPIO50		Unused	P5	19
FANIN1/GPIO51		Unused	P8	19
FANIN2/GPIO52		Unused	E9	19
TEMPIN0/GPIO61		Unused	B6	19
TEMPIN1/GPIO62		Unused	A6	19
TEMPIN2/GPIO63		Unused	A5	19
TEMPIN3/TALERT#/GPIO64		TALERT#	B5	19
VIN0/GPIO53		BIO5_WP#1	A4	19
VIN1/GPIO54		BIO5_WP#2	B4	19
VIN2/GPIO55		CLR_COMS	C4	19
VIN3/GPIO56		LAN_DISABLE	D4	19
VIN4/GPIO57		Unused	D5	19
VIN5/GPIO58		Unused	D6	19
VIN6/GPIO59		Unused	A7	19
VIN7/GPIO60		Unused	B7	19

Super I/O GPIO Config

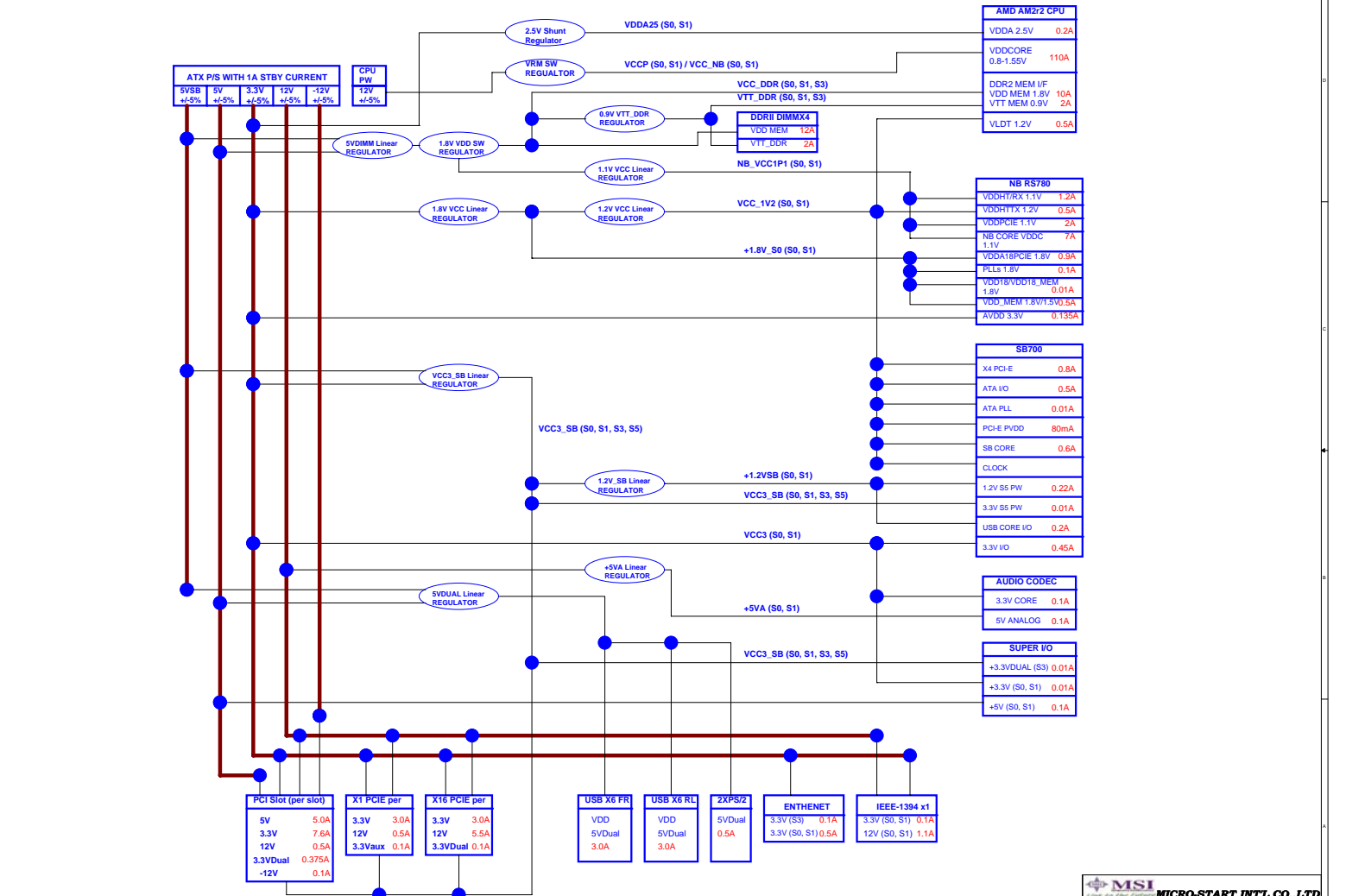
GPIO Name	Type	Function Description	Pin	Page
VIDO5/GP27		LEO_GPIO2	20	26
VIDO4/GP26		LEO_GPIO1	21	26
VIDO1/GP21/VGP0		LEO_GPIO0	26	26
PME#/GP54		LPC_PME#	73	26
KRST#/GP62		KBRST#	45	26
GA20/JP7		A20GATE	46	26
KDAT/GP61		KBDATA	80	26
KCLK/GP60		KBCLK	81	26
MDAT/GP57		MSDATA	82	26
MCLK/GP56		MSCLK	83	26
SUSC#/GP53		LPC_SM#	77	26
PSON#/GP42		PS_ON#	76	26
PANSWH#/GP43		PSIN	75	26
PWRON#/GP44		SB_PWRON#	72	26
PCIRST3#/GP11		ASSID_GPIO0	34	26
PCIRST2#/GP12		ASSID_GPIO1	33	26
FAN_TAC3/GP36		PWRFAN_PWM	12	26
FAN_TAC3/GP37		PWRFAN_TAC	11	26
FAN_CTL2/GP51		SYSFAN_PWM	10	26
FAN_TAC2/GP52		SYSFAN_TAC	9	26
FAN_CTL1		CPUFAN_PWM	8	26
FAN_TAC1		CPUFAN_TAC	7	26
VID2/GP32		COM_GPIO2	17	26
VID3/GP33		FUSB_G1	16	26
VID4/GP34		FUSB_G2	14	26
VID5/GP35		FUSB_G3	13	26

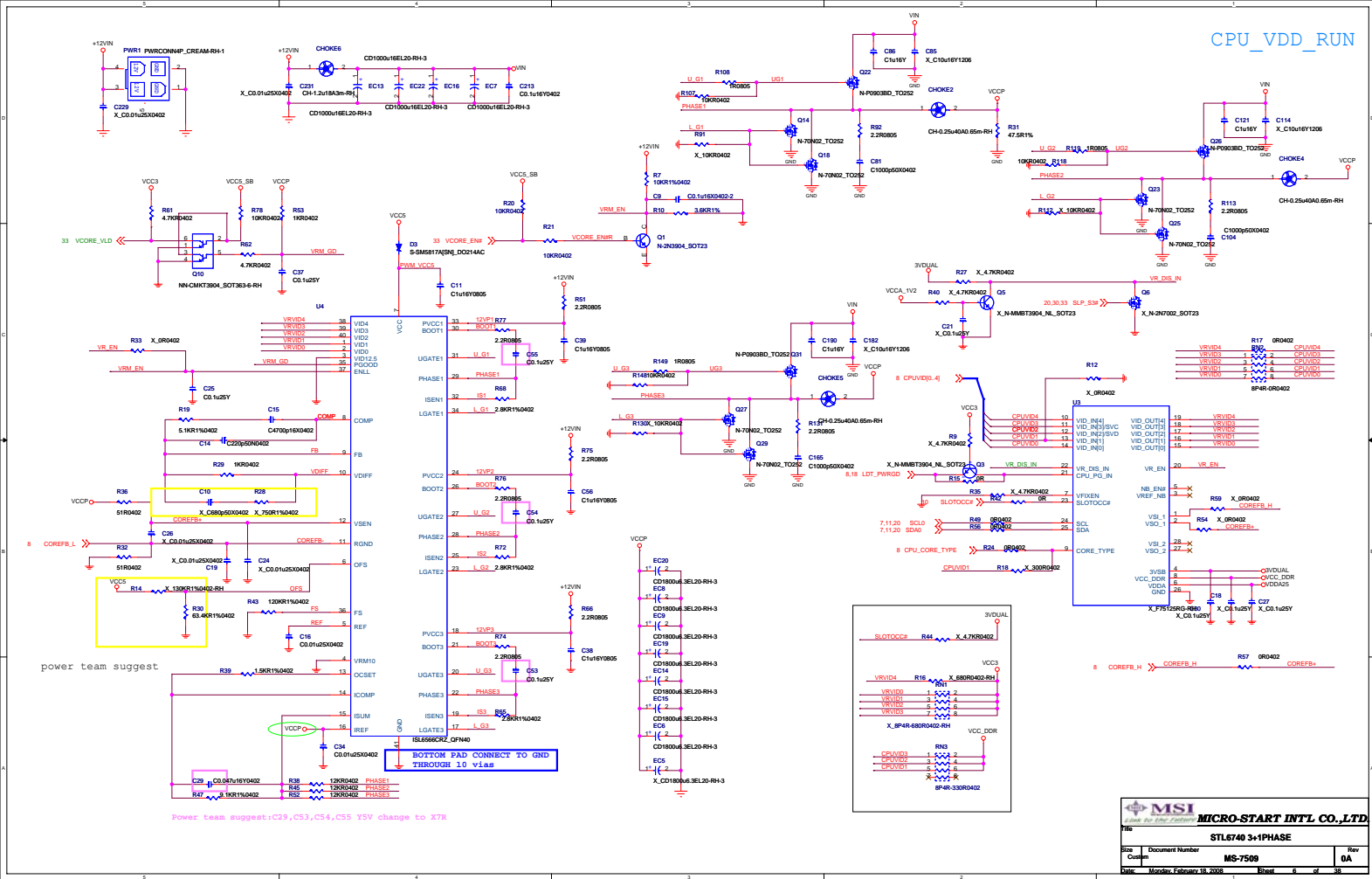
PCI Config.

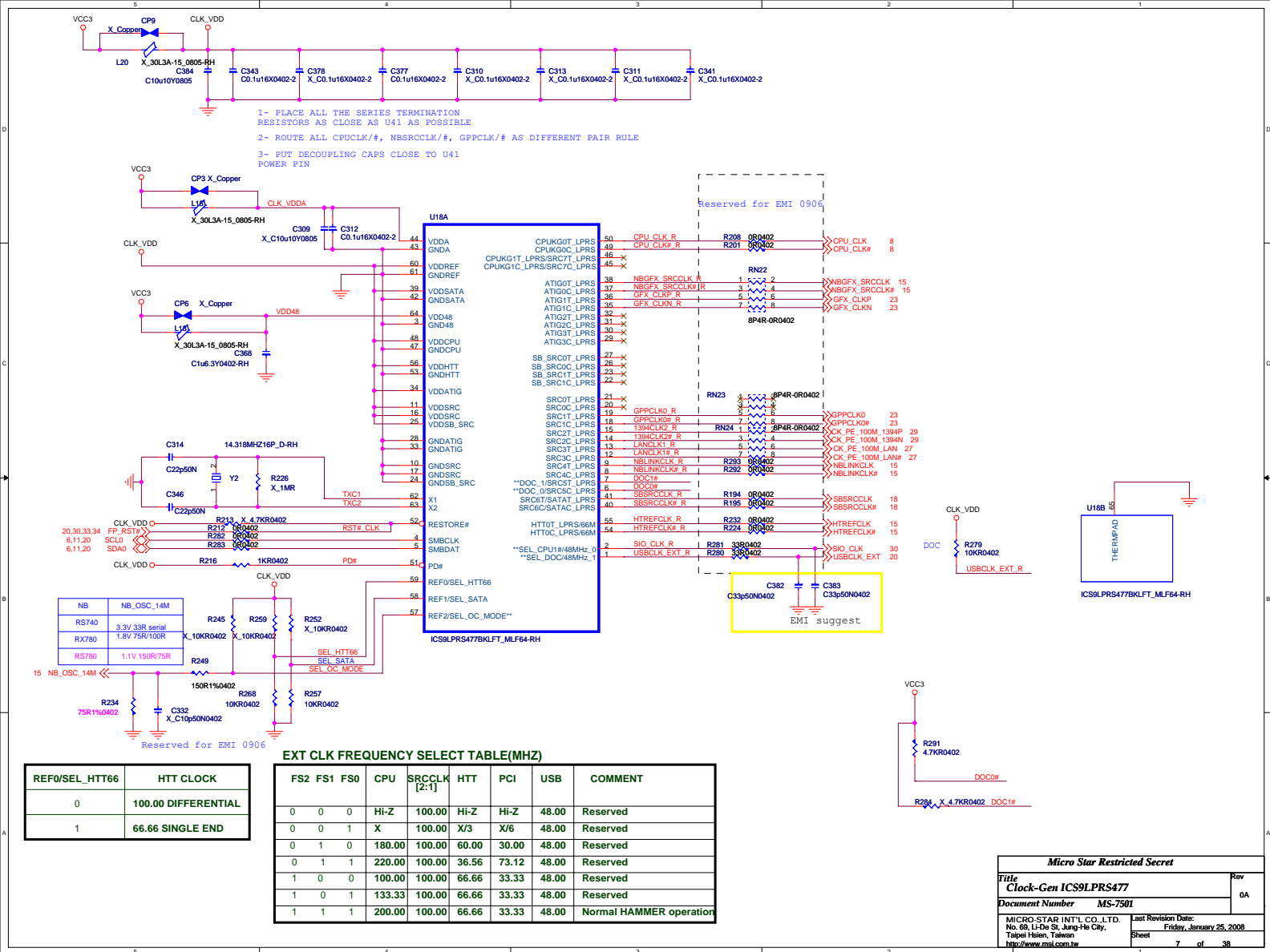
DEVICE	MCP1 INT Pin	REQ# / GNT#	IDSEL	CLOCK
PCI Slot 1	PC1_INTA#	PREQ#0 PGNT#0	AD16	PCICLK0
	PC1_INTB#			
	PC1_INT#			
	PC1_INTD#			
PCI Slot 2	PC1_INTB#	PREQ#1 PGNT#1	AD17	PCICLK1
	PC1_INT#			
	PC1_INTD#			
	PC1_INTA#			



Power Deliver Chart



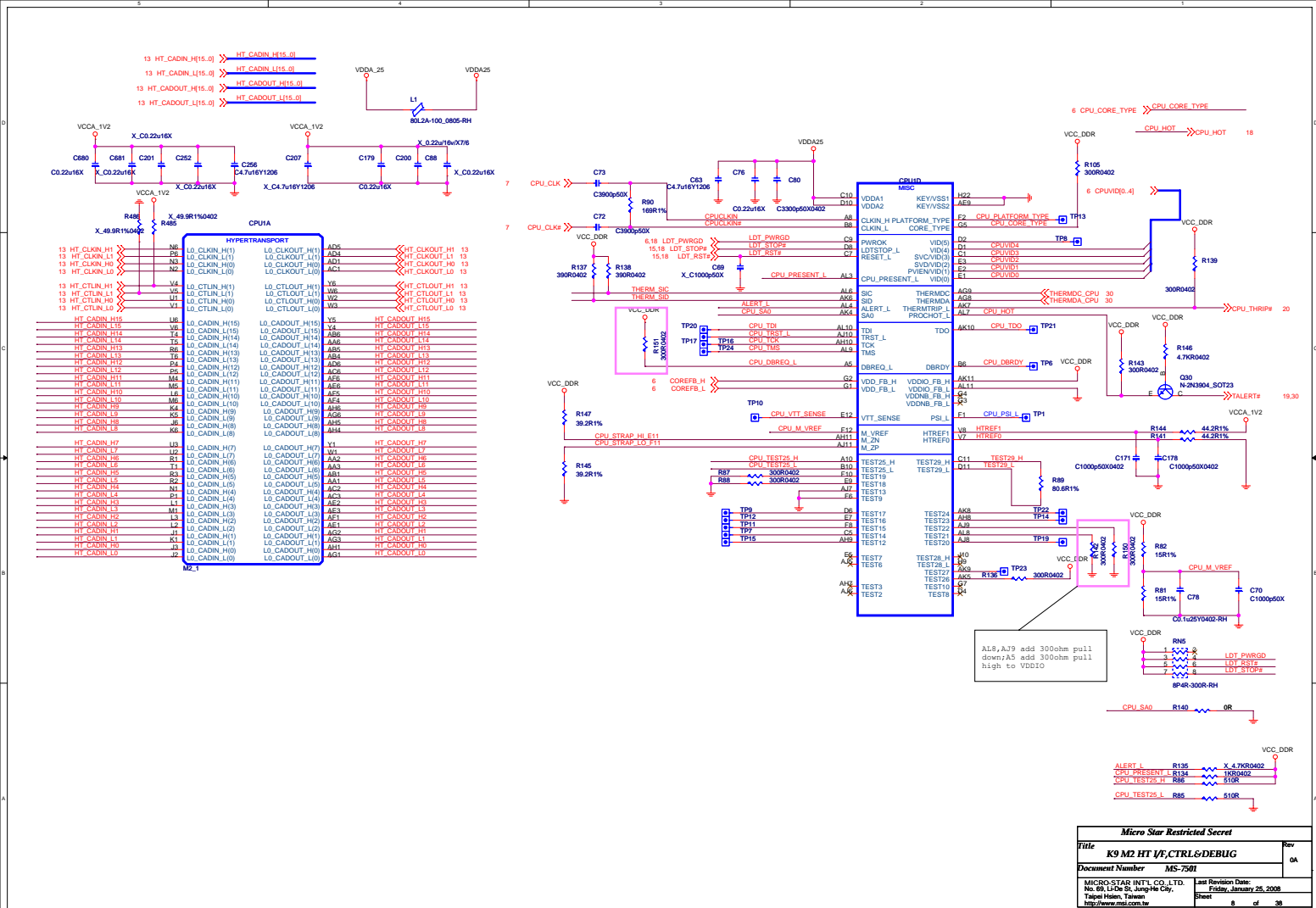




REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal HAMMER operation




```

11 MEM_MB_DQS_L[7..0] >> MEM_MB_DQS_L[7..0]
11 MEM_MB_DQS_H[7..0] >> MEM_MB_DQS_H[7..0]
11 MEM_MB_DM[7..0] >> MEM_MB_DM[7..0]
11,12 MEM_MB_ADD[15..0] >> MEM_MB_ADD[15..0]
.. MEM_MB_DATA[3..0]

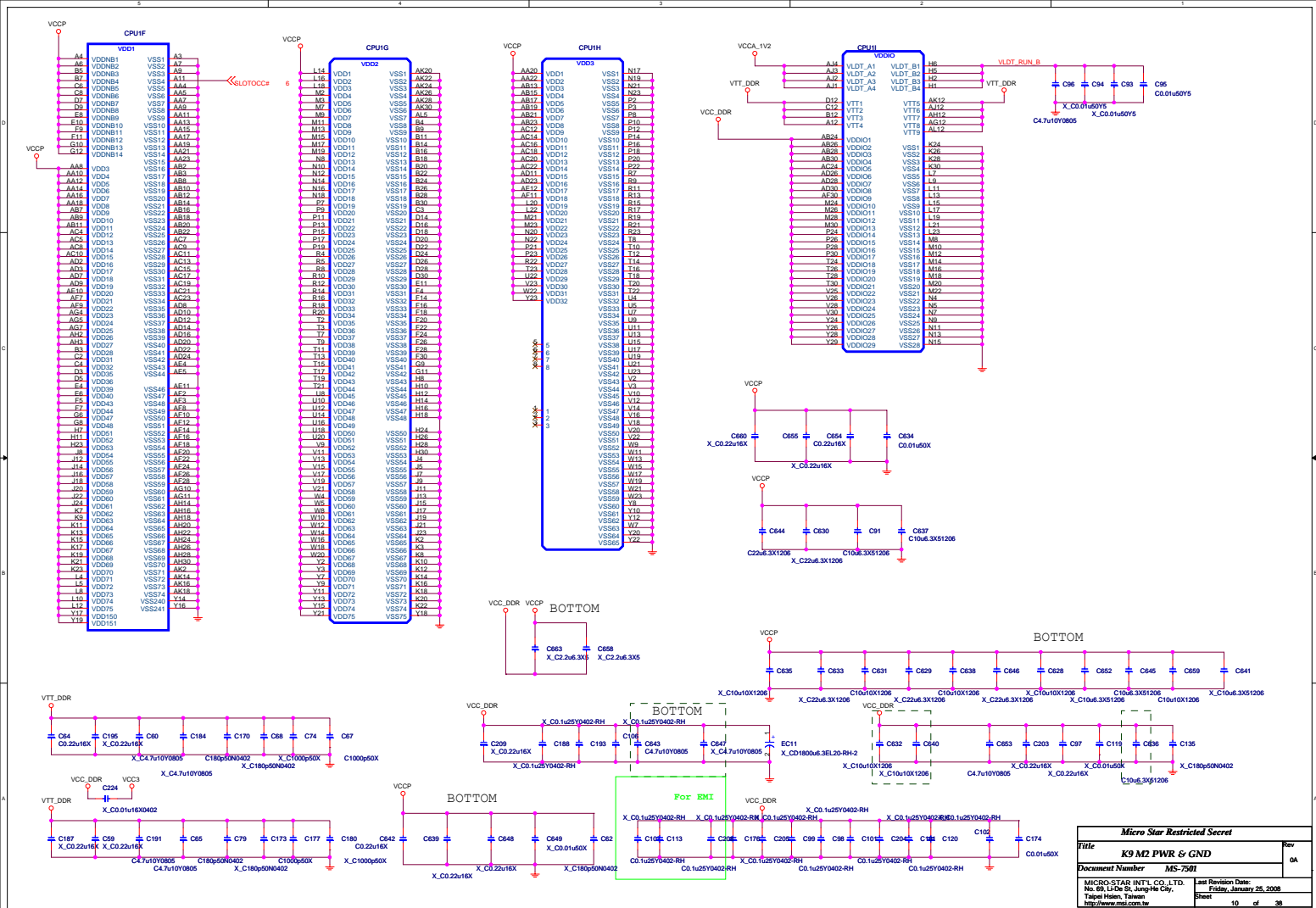
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CPU1B

		MEMORY INTERFACE A	
11:12	MEM_MAO_CLK_H2	MEM_MAO_CLK_H2	AG21
11:12	MEM_MAO_CLK_L2	MEM_MAO_CLK_L2	AG22
11:12	MEM_MAO_CLK_L1	MEM_MAO_CLK_L1	H10
11:12	MEM_MAO_CLK_H1	MEM_MAO_CLK_H1	H11
11:12	MEM_MAO_CLK_L0	MEM_MAO_CLK_L0	L26
11:12	MEM_MAO_CS_L1	MEM_MAO_CS_L1	AC29
11:12	MEM_MAO_CS_L0	MEM_MAO_CS_L0	AC30
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC38
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC39
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC40
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC41
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC42
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC43
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC44
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC45
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC46
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC47
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC48
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC49
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC50
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC51
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC52
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC53
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC54
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC55
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC56
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC57
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC58
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC59
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC60
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC61
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC62
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC63
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC64
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC65
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC66
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC67
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC68
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC69
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC70
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC71
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC72
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC73
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC74
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC75
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC76
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC77
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC78
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC79
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC80
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC81
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC82
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC83
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC84
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC85
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC86
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC87
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC88
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC89
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC90
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC91
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC92
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC93
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC94
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC95
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC96
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC97
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC98
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC99
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC100
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC101
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC102
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC103
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC104
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC105
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC106
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC107
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC108
11:12	MEM_MAO_ODT0	MEM_MAO_ODT0	AC109
11:12	MEM		

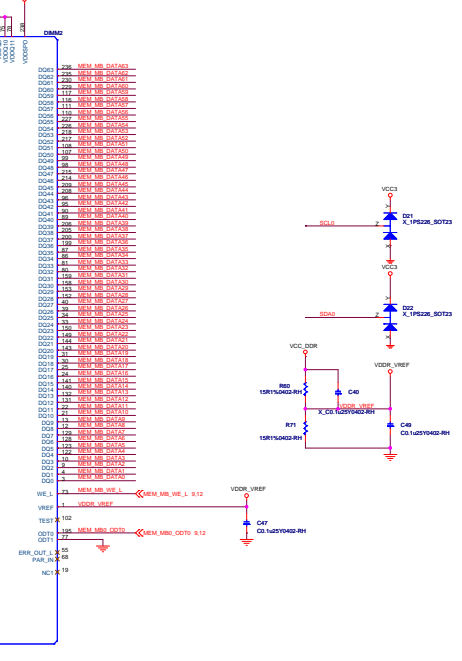
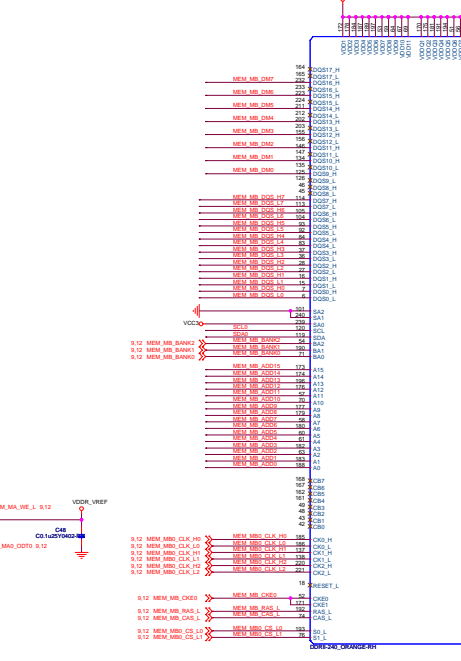
CPU1C

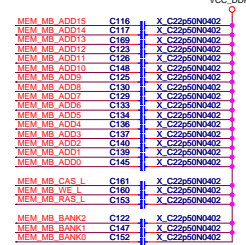
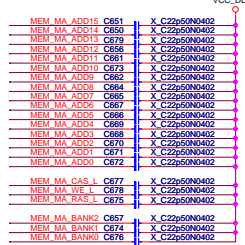
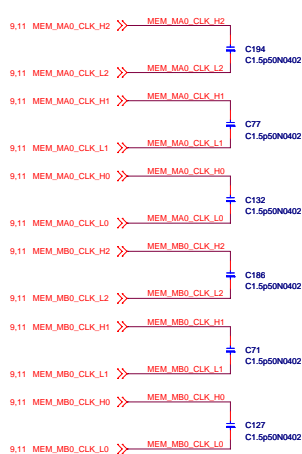
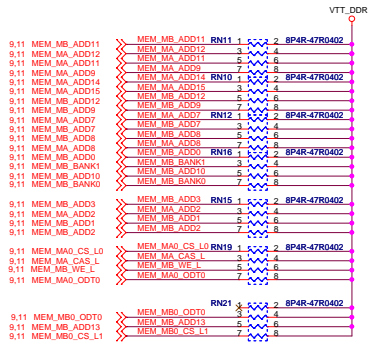
MEMORY INTERFACE 8					
11:12 MEM_MBO_CLK_H2	MEM_MBO_CLK_H2	A118	MEM_DAT8R3	A113	MEM_MBO_DAT8M5
11:12 MEM_MBO_CLK_L2	MEM_MBO_CLK_L2	A038	MEM_CLK_H2G2	A13	MEM_MBO_DAT8M6
11:12 MEM_MBO_CLK_H1	MEM_MBO_CLK_H1	A1	MEM_CLK_H1G1	DAB1	MEM_MBO_DAT8M7
11:12 MEM_MBO_CLK_L1	MEM_MBO_CLK_L1	A0	MEM_CLK_L1G1	A15	MEM_MBO_DAT8M8
11:12 MEM_MBO_CLK_H0	MEM_MBO_CLK_H0	U31	MEM_CLK_L1G2	A13	MEM_MBO_DAT8M9
11:12 MEM_MBO_CLK_L0	MEM_MBO_CLK_L0	U30	MEM_DAT8A5	A13	MEM_MBO_DAT8M10
			MEM_DAT8A6	A14	MEM_MBO_DAT8M7
			MEM_DAT8A7	A15	MEM_MBO_DAT8M8
11:12 MEM_MBO_CS_L1	MEM_MBO_CS_L1	A031	MEM_DAT8A8	A16	MEM_MBO_DAT8M9
11:12 MEM_MBO_CS_L0	MEM_MBO_CS_L0	AC0	MEM_DAT8A9	A17	MEM_MBO_DAT8M10
			MEM_DAT8A10	A18	MEM_MBO_DAT8M11
11:12 MEM_MBO_C0T0	MEM_MBO_C0T0	AD0	MEM_DAT8A11	A17	MEM_MBO_DAT8M12
			MEM_DAT8A12	A18	MEM_MBO_DAT8M13
			MEM_DAT8A13	A19	MEM_MBO_DAT8M14
			MEM_DAT8A14	A16	MEM_MBO_DAT8M15
			MEM_DAT8A15	A17	MEM_MBO_DAT8M16
			MEM_DAT8A16	A18	MEM_MBO_DAT8M17
			MEM_DAT8A17	A19	MEM_MBO_DAT8M18
			MEM_DAT8A18	A16	MEM_MBO_DAT8M19
			MEM_DAT8A19	A17	MEM_MBO_DAT8M20
			MEM_DAT8A20	A18	MEM_MBO_DAT8M21
			MEM_DAT8A21	A19	MEM_MBO_DAT8M22
			MEM_DAT8A22	A16	MEM_MBO_DAT8M23
			MEM_DAT8A23	A17	MEM_MBO_DAT8M24
			MEM_DAT8A24	A18	MEM_MBO_DAT8M25
			MEM_DAT8A25	A19	MEM_MBO_DAT8M26
			MEM_DAT8A26	A16	MEM_MBO_DAT8M27
			MEM_DAT8A27	A17	MEM_MBO_DAT8M28
			MEM_DAT8A28	A18	MEM_MBO_DAT8M29
			MEM_DAT8A29	A19	MEM_MBO_DAT8M30
			MEM_DAT8A30	A16	MEM_MBO_DAT8M31
			MEM_DAT8A31	A17	MEM_MBO_DAT8M32
			MEM_DAT8A32	A18	MEM_MBO_DAT8M33
			MEM_DAT8A33	A19	MEM_MBO_DAT8M34
			MEM_DAT8A34	A16	MEM_MBO_DAT8M35
			MEM_DAT8A35	A17	MEM_MBO_DAT8M36
			MEM_DAT8A36	A18	MEM_MBO_DAT8M37
			MEM_DAT8A37	A19	MEM_MBO_DAT8M38
			MEM_DAT8A38	A16	MEM_MBO_DAT8M39
			MEM_DAT8A39	A17	MEM_MBO_DAT8M40
			MEM_DAT8A40	A18	MEM_MBO_DAT8M41
			MEM_DAT8A41	A19	MEM_MBO_DAT8M42
			MEM_DAT8A42	A16	MEM_MBO_DAT8M43
			MEM_DAT8A43	A17	MEM_MBO_DAT8M44
			MEM_DAT8A44	A18	MEM_MBO_DAT8M45
			MEM_DAT8A45	A19	MEM_MBO_DAT8M46
			MEM_DAT8A46	A16	MEM_MBO_DAT8M47
			MEM_DAT8A47	A17	MEM_MBO_DAT8M48
			MEM_DAT8A48	A18	MEM_MBO_DAT8M49
			MEM_DAT8A49	A19	MEM_MBO_DAT8M50
			MEM_DAT8A50	A16	MEM_MBO_DAT8M51
			MEM_DAT8A51	A17	MEM_MBO_DAT8M52
			MEM_DAT8A52	A18	MEM_MBO_DAT8M53
			MEM_DAT8A53	A19	MEM_MBO_DAT8M54
			MEM_DAT8A54	A16	MEM_MBO_DAT8M55
			MEM_DAT8A55	A17	MEM_MBO_DAT8M56
			MEM_DAT8A56	A18	MEM_MBO_DAT8M57
			MEM_DAT8A57	A19	MEM_MBO_DAT8M58
			MEM_DAT8A58	A16	MEM_MBO_DAT8M59
			MEM_DAT8A59	A17	MEM_MBO_DAT8M60
			MEM_DAT8A60	A18	MEM_MBO_DAT8M61
			MEM_DAT8A61	A19	MEM_MBO_DAT8M62
			MEM_DAT8A62	A16	MEM_MBO_DAT8M63
			MEM_DAT8A63	A17	MEM_MBO_DAT8M64
			MEM_DAT8A64	A18	MEM_MBO_DAT8M65
			MEM_DAT8A65	A19	MEM_MBO_DAT8M66
			MEM_DAT8A66	A16	MEM_MBO_DAT8M67
			MEM_DAT8A67	A17	MEM_MBO_DAT8M68
			MEM_DAT8A68	A18	MEM_MBO_DAT8M69



9 MEM_MBA_DQS_167-18 MEM_MBA_DQS_167-18
9 MEM_MBA_DQS_167-18 MEM_MBA_DQS_167-18
9 MEM_MBA_DQS_167-18 MEM_MBA_DQS_167-18
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9 MEM_MBA_DQS_167-18 MEM_MBA_DQS_167-18

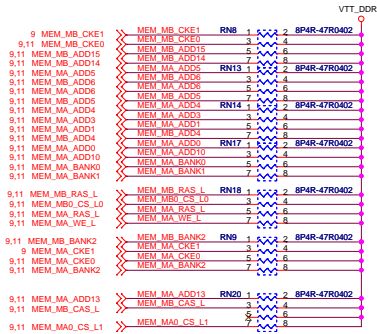
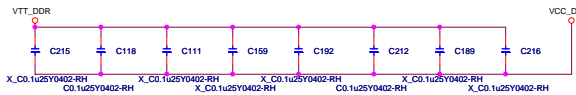
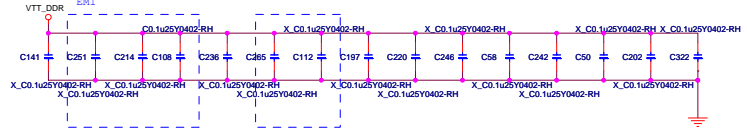
9 MEM_MBA_DQS_167-18 MEM_MBA_DQS_167-18
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9 MEM_MBA_DQS_167-18 MEM_MBA_DQS_167-18
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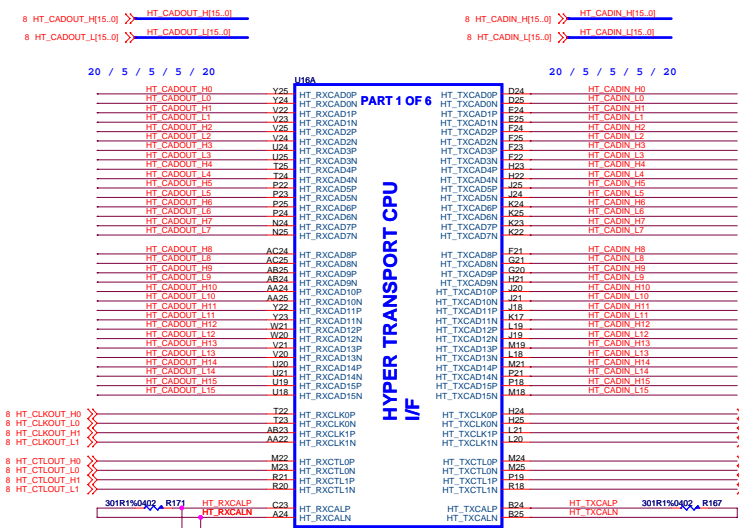
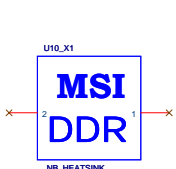




Decoupling Between Processor and DIMMs

Layout: Spread out on VTT pour





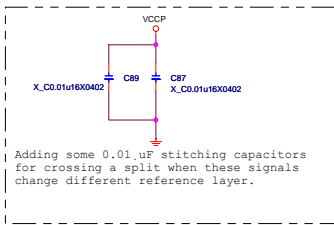
PART 1 OF 6

HYPER TRANSPORT CPU
I/F

Check U10 New Version : Port Number

RX780/RS740/RS780 difference table (HT LINK)

SIGNALS	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)		
HT_TXCALP	100R	1.21K	301R
HT_TXCALN			



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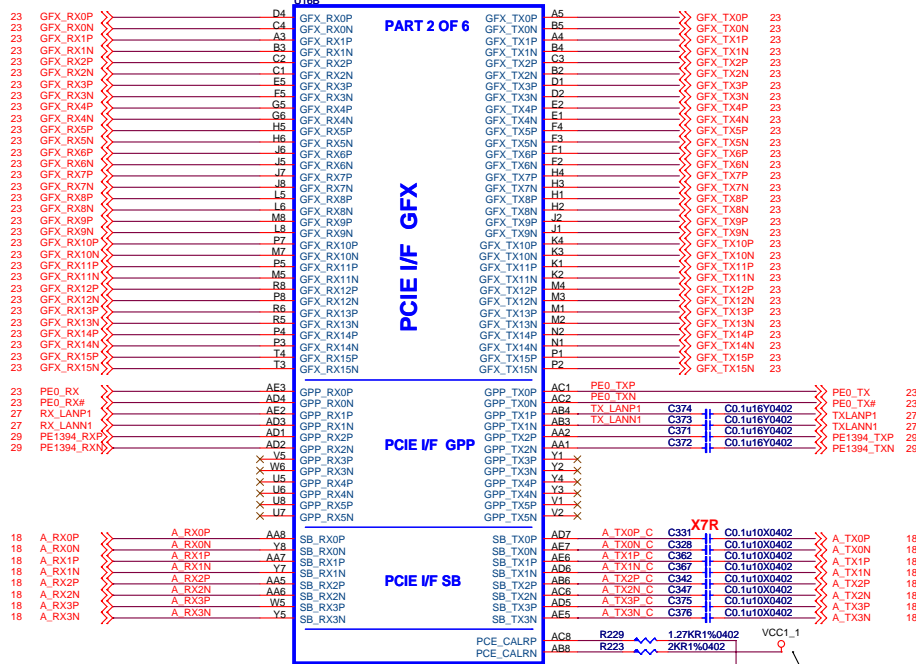
File RS780-HT L

Size Document Number MS-7501 Rev 0A

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20 / 5.5 / 4.5 / 5.5 / 20

20 / 5.5 / 4.5 / 5.5 / 20



AMD-215-0674007-00-A01-RH

RX780/RS740/RS780 GPP difference table

	RS740	RX780/RS780
PCE_CALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RS780 Display Port Support (muxed on GFX)

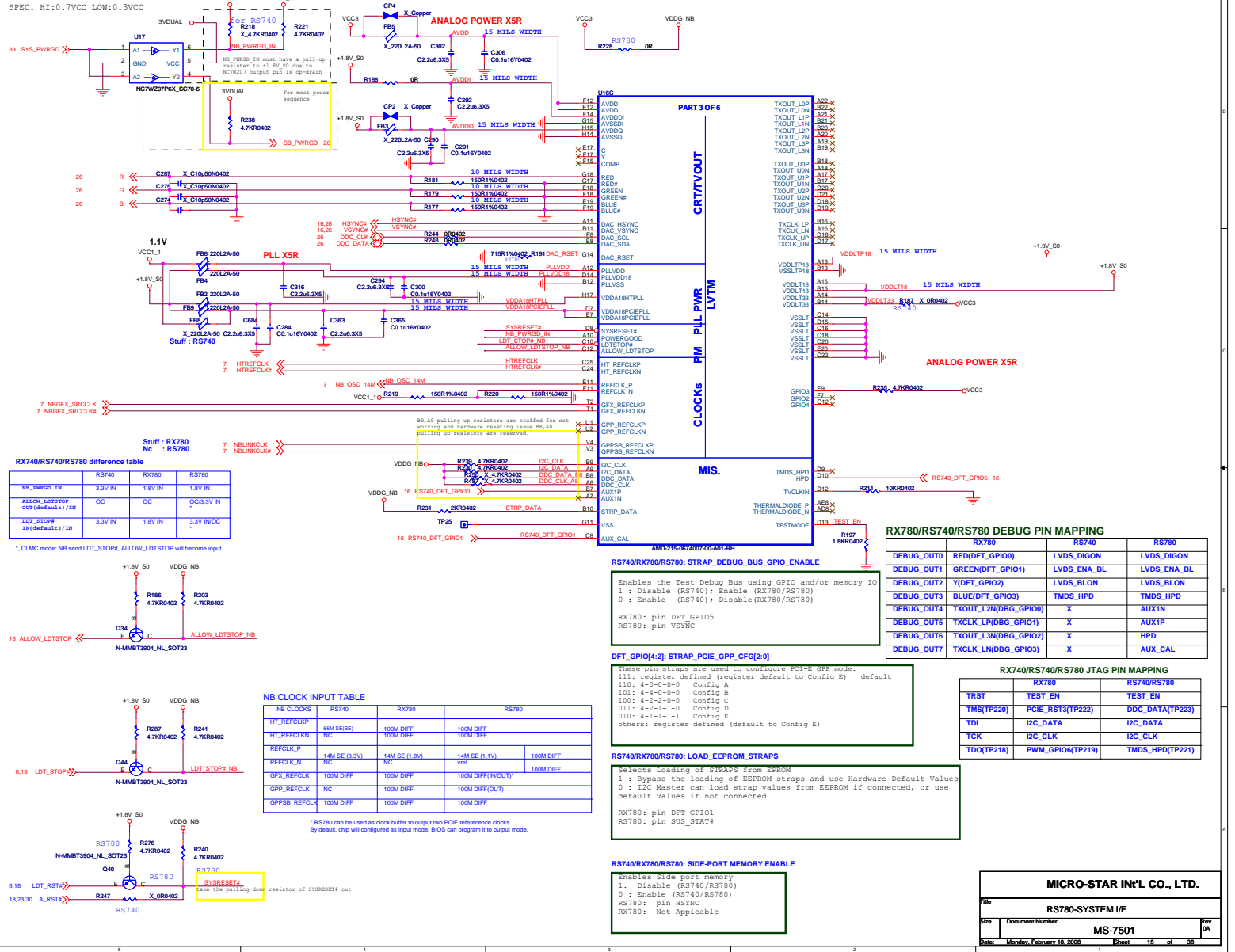
DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

RX780/RS740/RS780 GPP Routing table

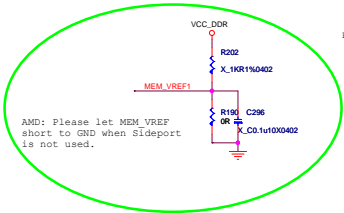
	RS740	RX780/RS780
GPP X4 CONNECTOR	GPP[2:0]	GPP[3:0]
GPP X1 CONNECTOR		GPP4
GIGABIT ETHERNET	GPP3	GPP5

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Title		
RS780-PCIE I/F		
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FOR RS780,R148,R162,C203 and C202 will be populated.

Note: for RS780, change R232 to 150R as AUX_CAL, place close to pin C8

45 R2340 DET CRIO1 R243 150R0402



RS740/RX780/RS780: SIDE-PORT MEMORY ENABLE



RX780/RS780: STRAP_DEBUG_BUS_PCIE_ENABLE



```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
  default values if not connected
RS740: pin DFT_GPIO1

RS780: pin SUS_STAT#
```

```
Enables the Test Debug Bus using GPIO and/or memory IO
1 : Disable (RS740/RS780); Enable (RX780)
0 : Enable (RS740/RS780); Disable (RX780)
RS740: pin DFT_GPIO5

RS780: pin VSYNC
```

```
Enables Side port memory
1. Disable (RS740/RS780)
0 : Enable (RS740/RS780)
RS740: pin DFT_GPIO0
RS780: pin HSYNC
```

```
Enables Test debug bus
using PCIE bus
1. Disable (can be enabled
   thru nbcfg register)
0 : Enable

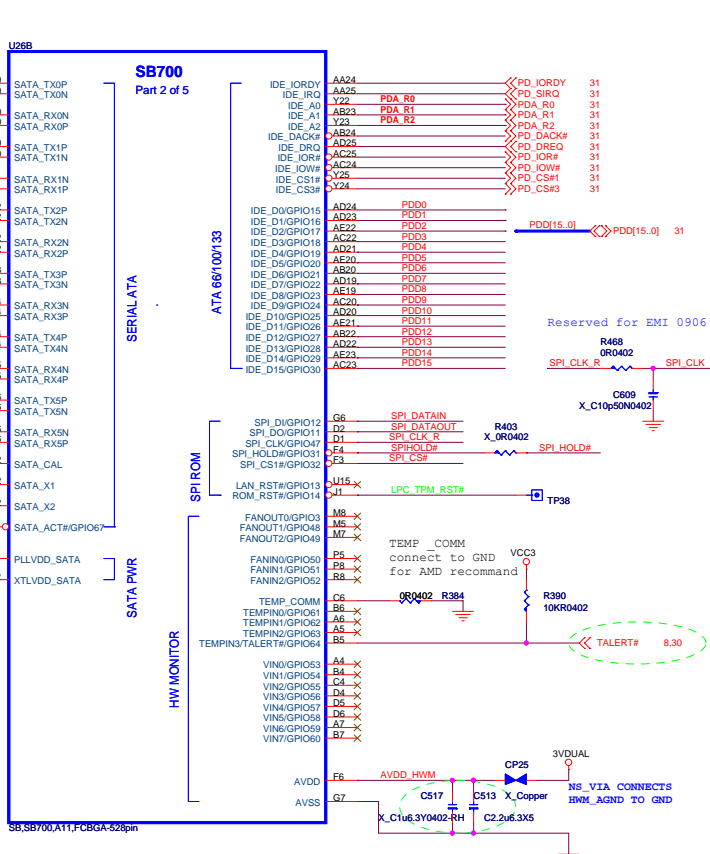
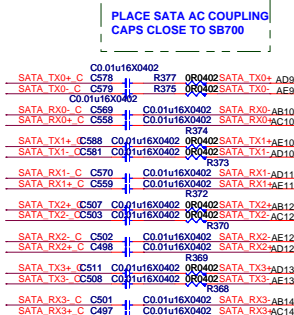
RS780: configurable thru register
       setting only
RS740: Not supported
```

Title				RS780-SPMEM/STRAPS			
Size	Document Number						Rev
	MS-7501						0A
Date	Monday, February 18, 2008			Sheet	16	of	38

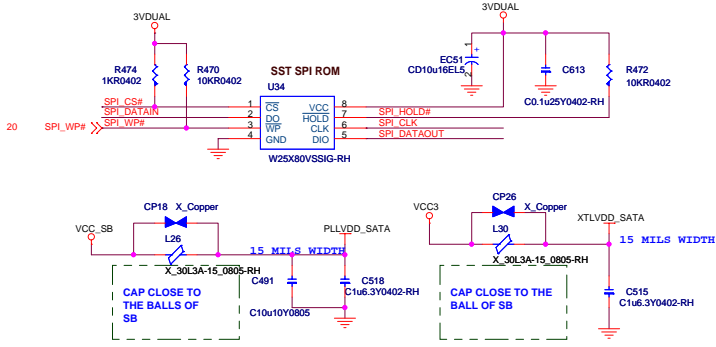
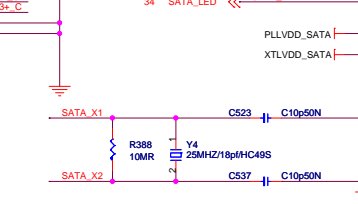


4 Ss 3 Ps
1 Pm 2 Sm

N5N-07M0231-H06



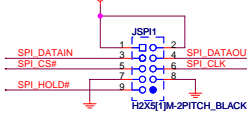
R272 IS 1K 1% FOR XTAL, 4.99K 1% FOR INTERNAL CLK



SPI FLASH MEMORY

SPI DEBUG PORT

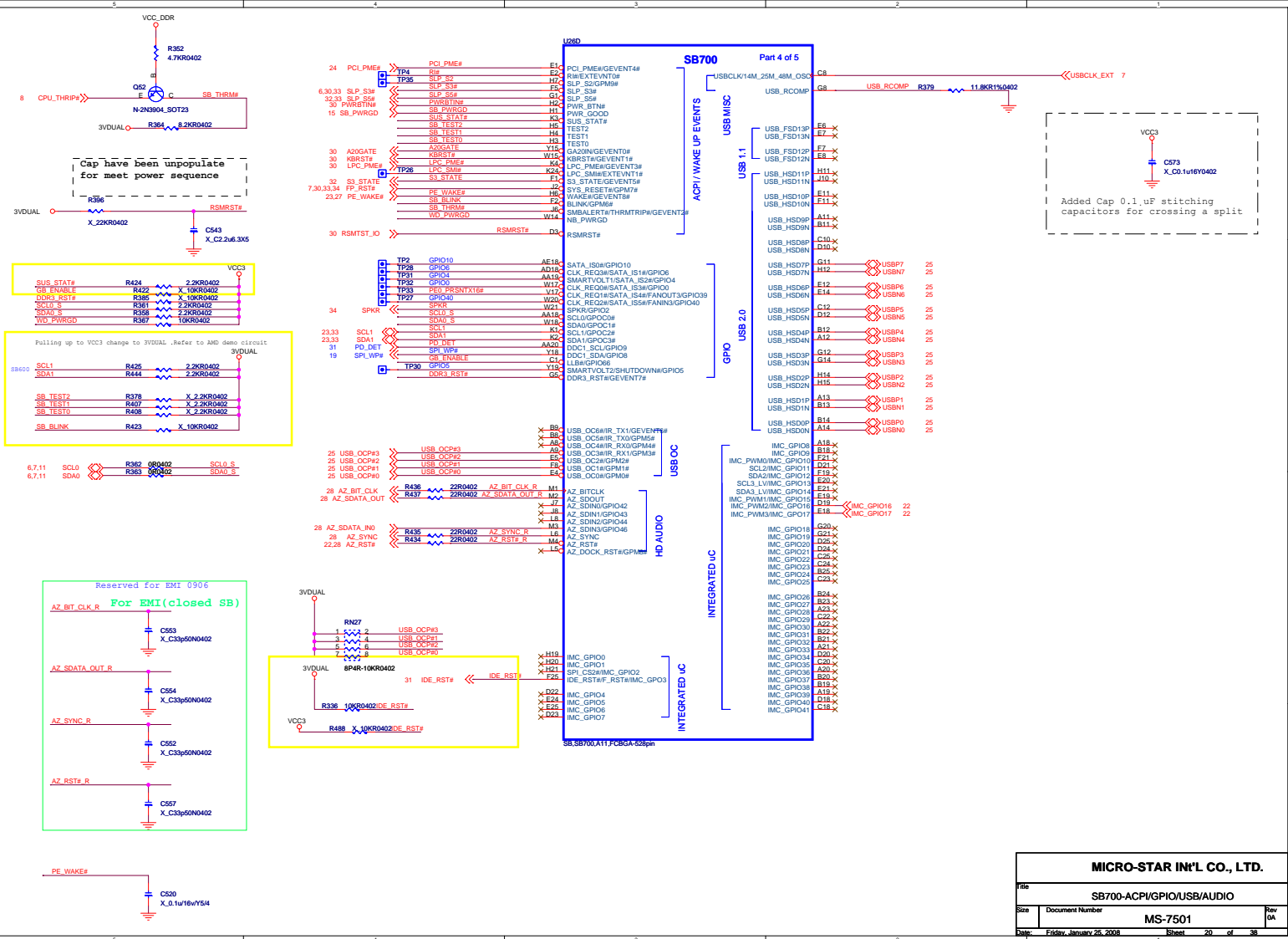
Place close to SPI ROM

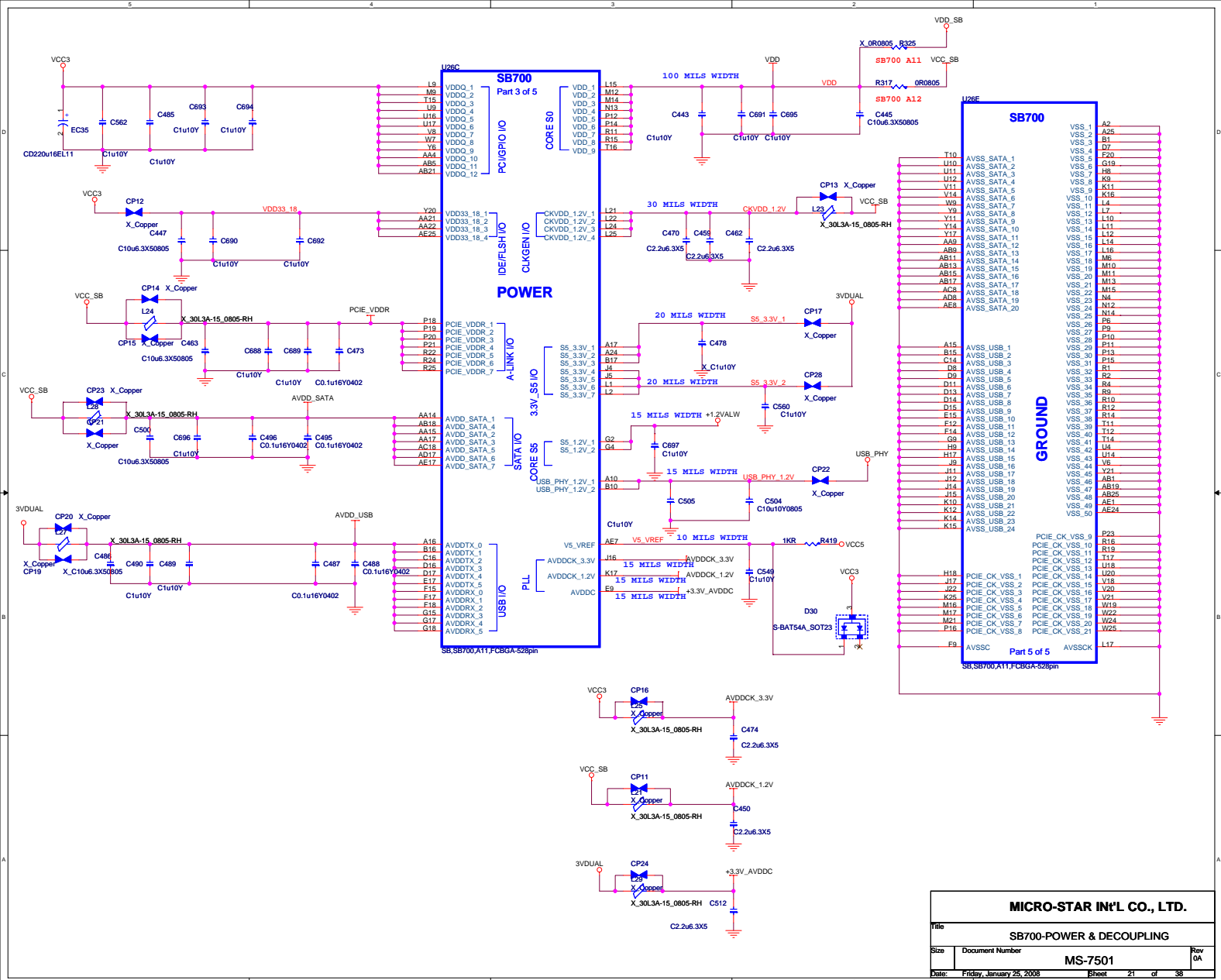


Part Number : N31-2051451-H06

MICRO-STAR INT'L CO., LTD.

Title			
SB700-SATA/IDE/HWM/SPI			
Size	Document Number	MS-7501	Rev 0A
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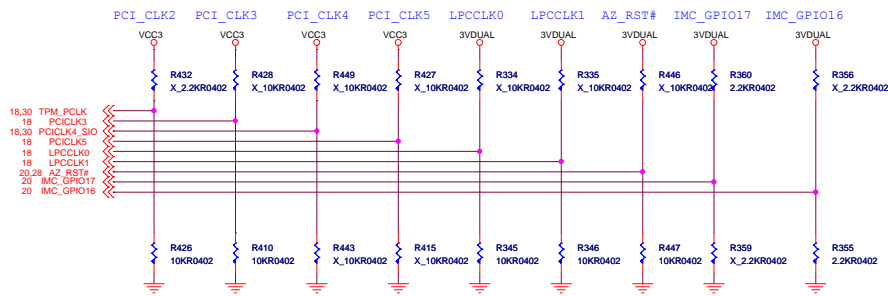






REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	AZ_RST#	IMC_GPIO17	IMC_GPIO16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	IMC ENABLED	ROM TYPE: H, H = Reserved L, L = SPI ROM	DEFAULT
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	IMC DISABLED DEFAULT	L, H = LPC ROM L, L = FWH ROM	

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[30:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

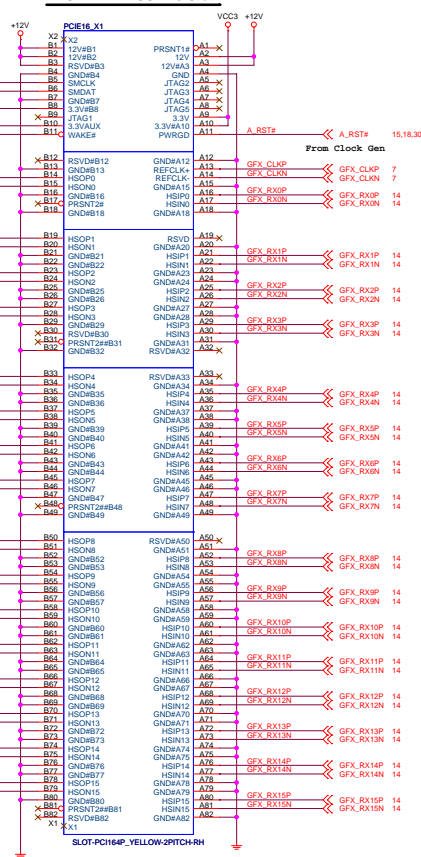
MICRO-STAR IN'L CO., LTD.

Title			SB700-STRAPS
Size	Document Number	MS-7501	
Date	Friday, January 25, 2008	Sheet	22 of 38

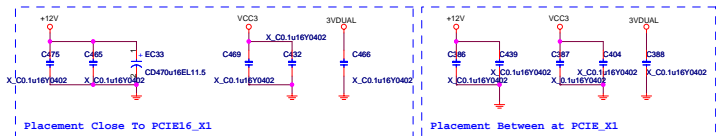
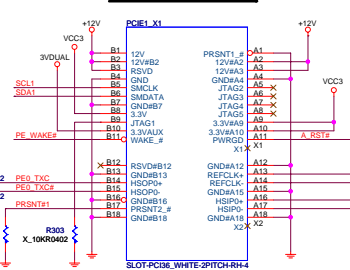
PCI Express Slot x16/x1



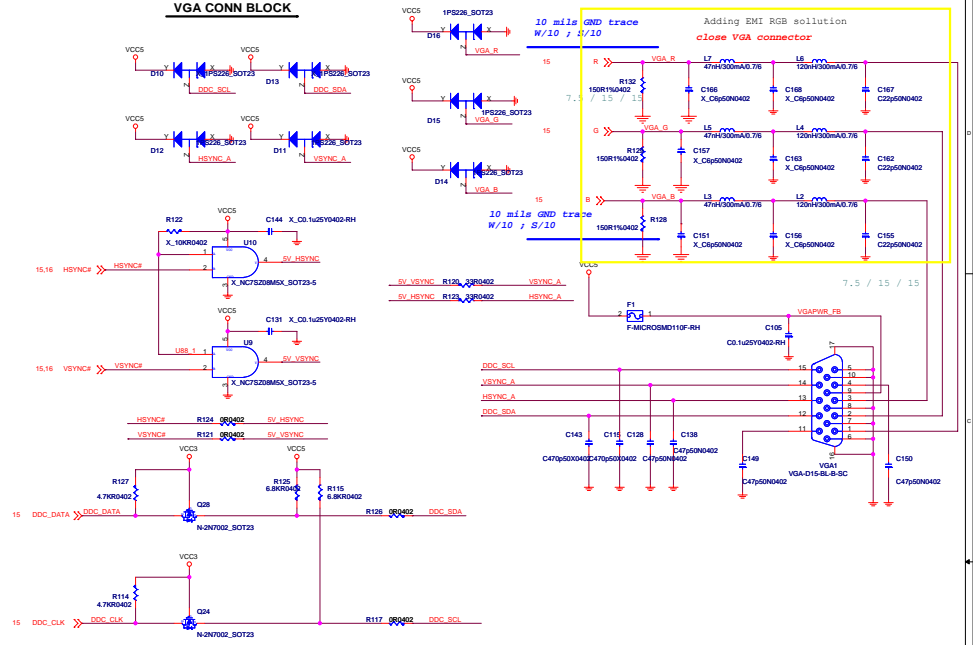
PCI EXPRESS x16 Slot



PCI EXPRESS 1 Slot-1

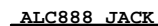


VGA CONN BLOCK



MICRO-STAR INC'L CO., LTD.			
File: VGA CONN / TVOUT			
Size	Document Number	MS-7501	Rev
Date	File	January 25, 2008	Sheet 26 of 26

883 :B09-LC88304-R09
888: B09-LC88804-R09
861D:B09-LC86124-R09

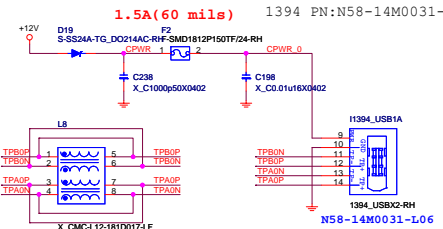


SPDIF_OUT

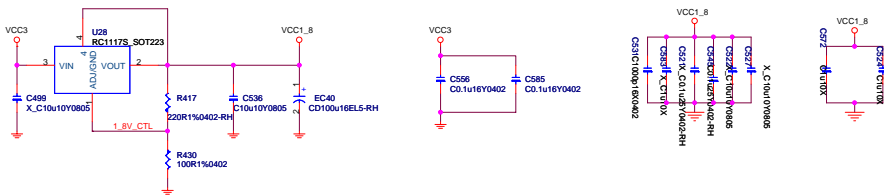
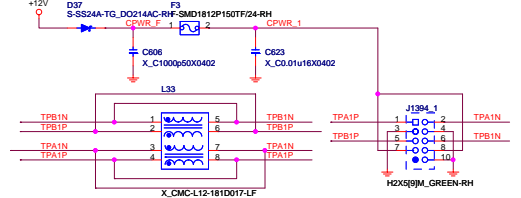


MICRO-STAR INT'L CO., LTD.	
Title	
ALC888 CO-LAY ALC883 CODEC	
Size	Document Number
	MS-7379
Date:	Friday, January 25, 2008
Sheet	28 of 38
Rev	3.0

No 1394 PN :N53-08M0191-A10
1394 PN:N58-14M0031-L06

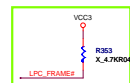


1.5A(60 mils)

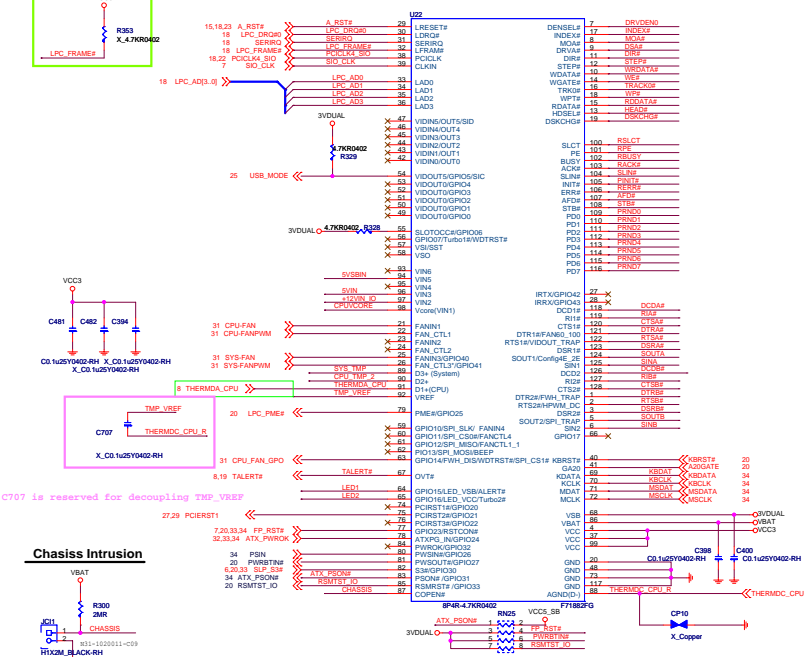


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Date:	Wednesday, January 30, 2008	Sheet 29 of 38	

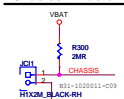
Super I/O



LPC SUPER I/O F71882



Chassis Intrusion

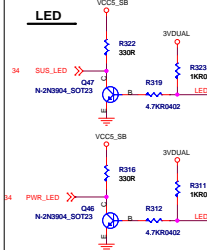


LPC I/O STRAPPING RESISTOR

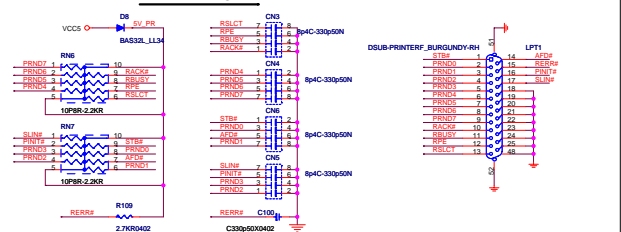


	Don't STUFF	STUFF
RTSB#	PWM FAN	LINEAR FAN
RTSA#	PIN49-54=VID_OUT	PIN49-54=GPIO
	PIN42-47=VIDIN	PIN42-47=VIDIN/OUT
SOUTA	4E	2E
OTRA#	FAN START DUTY 60%	FAN START DUTY 100%

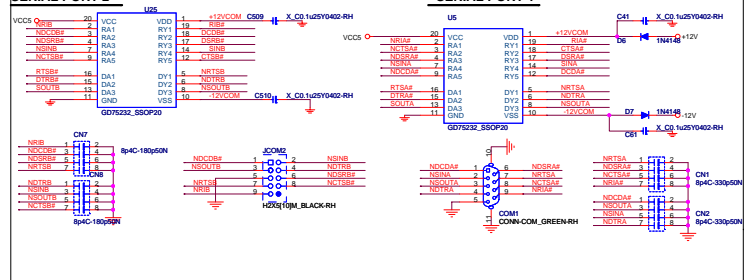
LED



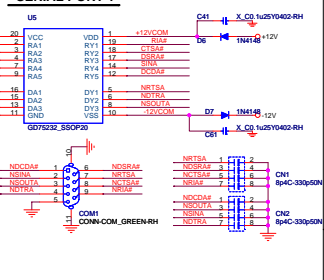
PARALLAL PORT



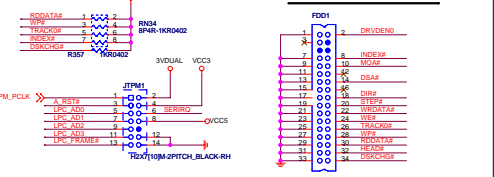
SERIAL PORT 2



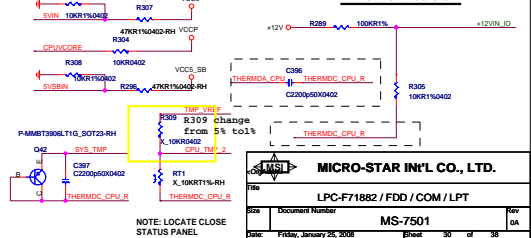
SERIAL PORT 1



FLOPPY CONNECTOR



Thermal Resistor



NOTE: LOCATE CLOSE


MICRO-STAR INT'L CO., LTD.

LPC-F71882 / FDD / COM / LPT

Size	Document Number
	MS-7501

Intel Front Panel

